

## FLOPPY DISK FORMATTER / CONTROLLER (FDC)

NOVEMBER 1980

### DESCRIPTION

The Fujitsu MB88XX family is a one-chip Floppy Disk Formatter/Controller (FDC) which is fabricated with N-channel E/D MOS technology.

The MB88XX can be applied to any of single density floppy disk, double density floppy disk and mini floppy disk.

The IBM3740 format and the frequency modulation (FM) recording are used for the single density storage, and the IBM System-34 format and the modified frequency modulation (MFM) recording are used for the double density storage.

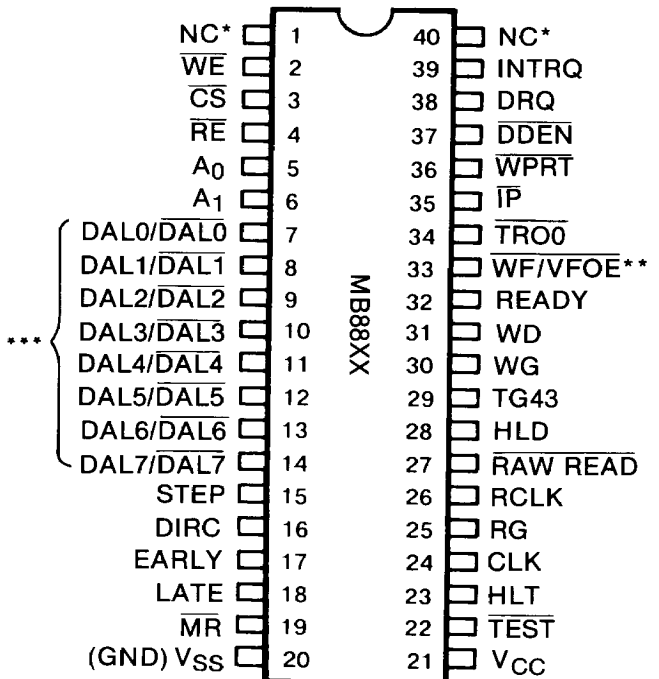
Also, the MB88XX interfaces with an 8-bit parallel microprocessor to control data transfer and mechanical operation. The MB88XX is packaged in a standard 40-pin dual-in-line-package.

- N-Channel E/D MOS Technology
- MB8866 Upward Compatible with Western Digital FD1791 ✓
- MB8876 Upward Compatible with Western Digital FD1791-01, FD1791-02 ✓
- MB8877 Upward Compatible with Western Digital FD1793

### FEATURES

- Single +5V Power Supply
- IBM Compatible Sector Format
- Automatic Track Seeking and Verification
- Both Single and Double Density Formats
  - a) Single Density in IBM3740 Format and FM Recording
  - b) Double Density in IBM System-34 Format and MFM Recording
- Programmable Single Sector/Multiple Sectors/Entire Track Read Operation
- Programmable Single Sector/Multiple Sectors/Entire Track Write Operation
- Programmable Side Compare Function Available MB8876 and MB8877
- Programmable Sector Length
- Programmable Head Step Rate
- Programmable Head Engage/Head Settle Time
- Double Buffered Data I/O
- DMA Data Transfer Capability
- Write Precompensation Capability
- All TTL Compatible I/O

### PIN ASSIGNMENT



PACKAGE

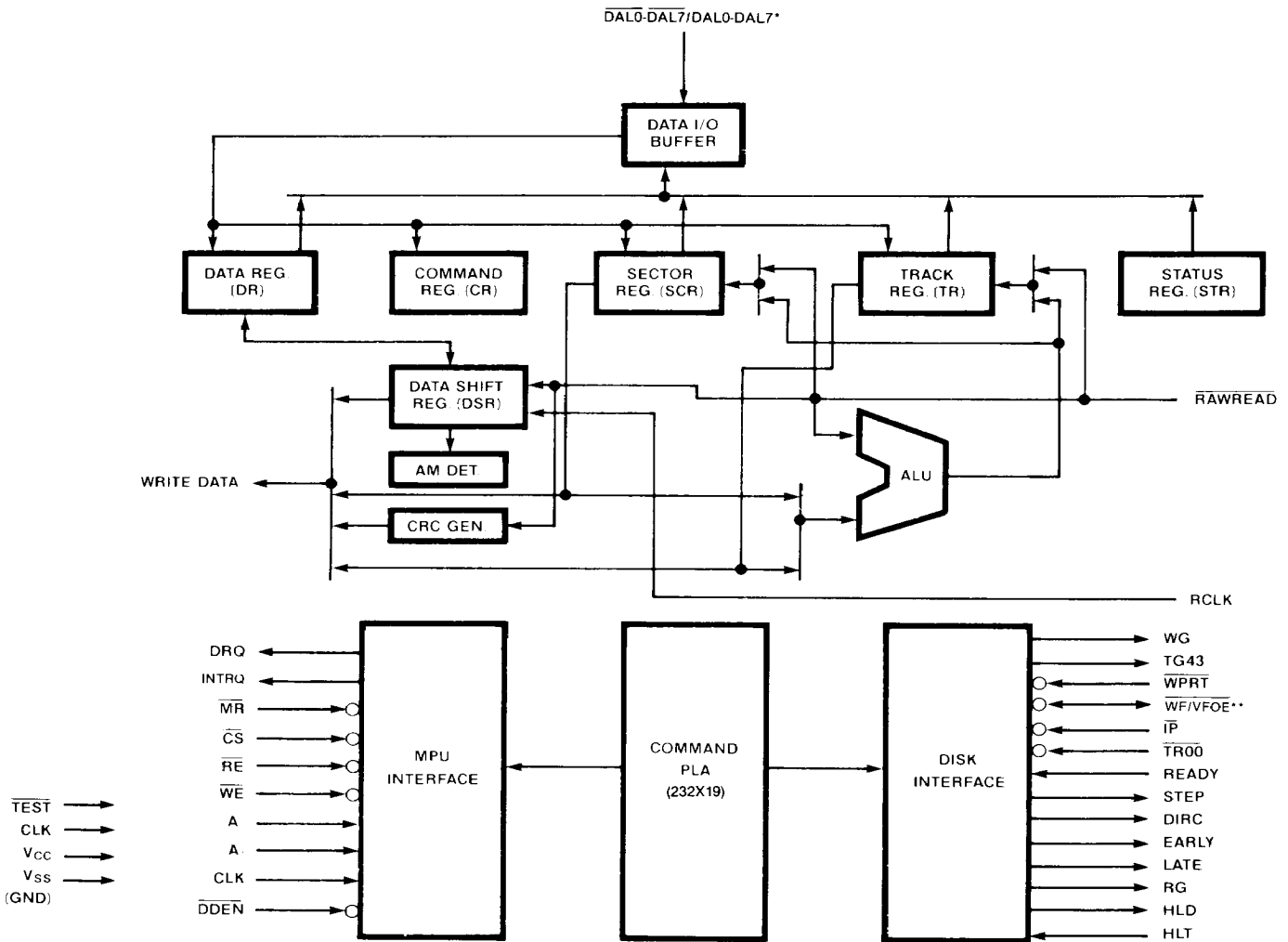
DIP-40C-A01

\*: No Connection

\*\* : MB8866 WF Only

\*\*\* { MB8876: Negative Logic  
MB8877: Positive Logic

MB8866 / MB8876 / MB8877 BLOCK DIAGRAM



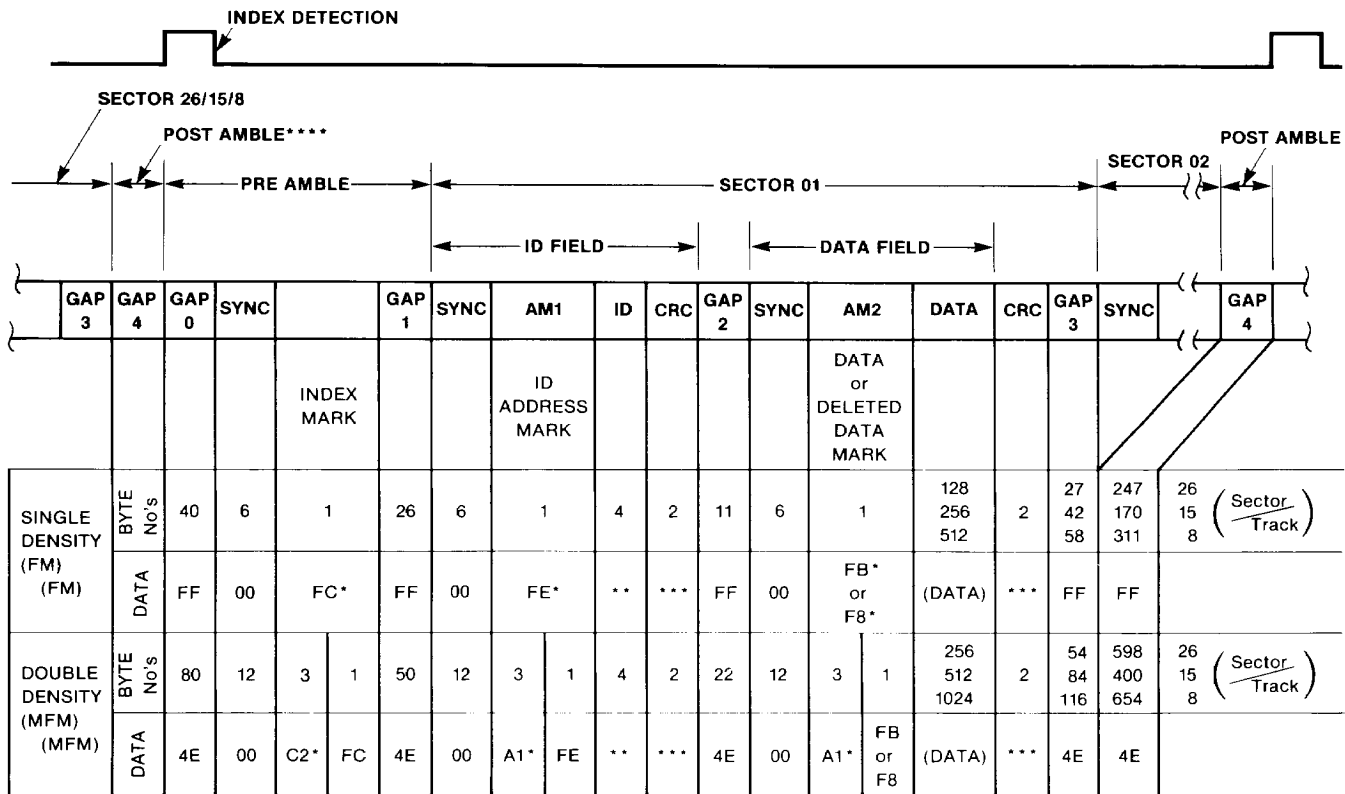
\*MB8877 TRUE DATA BUS  
 \*\*MB8866 WF ONLY

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on any pin to V <sub>SS</sub>	V <sub>CC</sub> , V <sub>I</sub> , V <sub>O</sub>	- 0.3 to + 7.0	V
Operating Temperature	T <sub>OP</sub>	0 to 70	°C
Storage Temperature	T <sub>stg</sub>	- 55 to + 150	°C
Power Dissipation	P <sub>D</sub>	800	mW

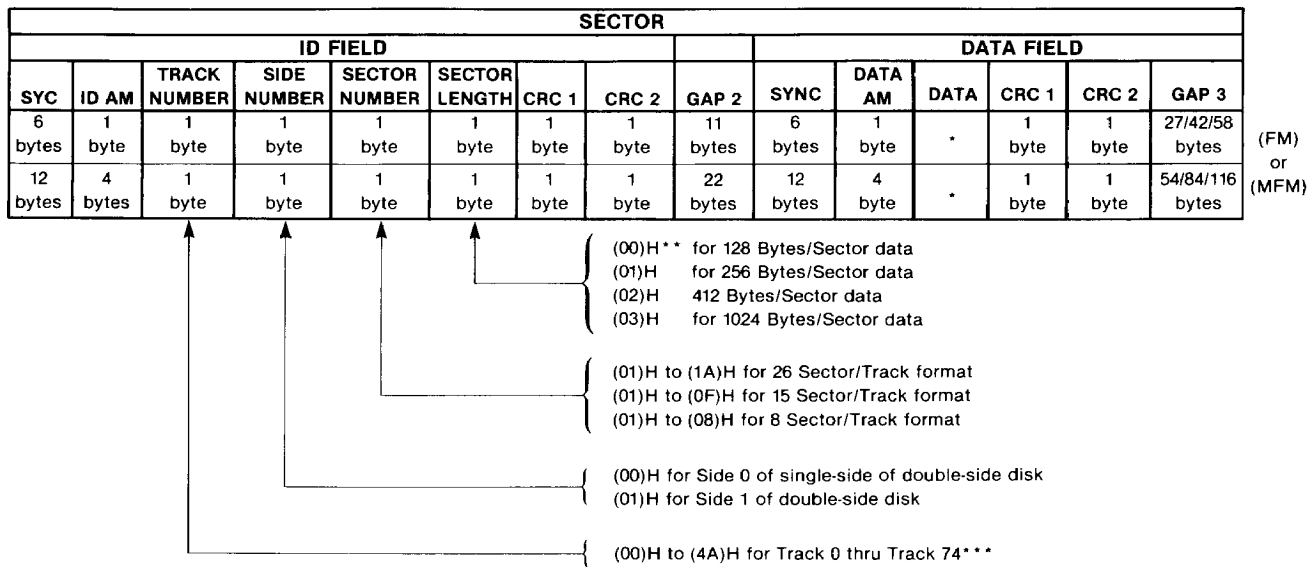
Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

**TRACK FORMAT**



**NOTE:** \*: Shows to have missing clock.  
 \*\*: Shows the ID field  
 \*\*\*: Shows the cyclic Redundancy check polynomial  $G(X) = X^6 + X^5 + X^{12} + X^{16}$   
 \*\*\*\*: See the most right column for its byte numbers and data.

**SECTOR FORMAT**



**NOTE** \*: Byte number of this column is defined in the SECTOR LENGTH column.  
 \*\*: "H" after parentheses show that the parenthesized figures are hexa-decimal.  
 \*\*\*: Track 75 and 76 are usually used for correction.

# MB8866 / MB8876 / MB8877

## PIN DESCRIPTIONS

### MPU Interface Pins

Pin 2,  $\overline{WE}$  (Write Enable)

This input is used as a strobe signal when data is written into internal registers.

When  $\overline{WE} = 0$  and  $CS = 0$ , data can be written into internal registers.

Pin 3,  $\overline{CS}$  (Chip Select)

This input is used for enabling this FDC device.

When  $\overline{CS} = 0$  this FDC device is selected and data transfer between this FDC device and an MPU is enabled.

Pin 4,  $\overline{RE}$  (Read Enable)

This input is used as a strobe signal when data is read from internal registers.

When  $\overline{RE} = 0$  and  $CS = 0$ , data can be read from internal registers.

Pin 5 and 6,  $A_0$  and  $A_1$  (Register Select Address)

These inputs are used to address an internal register among the Command Register (CR), Status Register (STR), Track Register (TR), Sector Register (SCR) and Data Register (DR). (Refer to Table 1.)

## REGISTER SELECTION

Chip Select	Address		Selected Register		Data Bus Status
	$A_1$	$A_0$	For Read Mode ( $\overline{RE} = 0$ )	For Write Mode ( $\overline{WE} = 0$ )	
$\overline{CS}$	$A_1$	$A_0$	For Read Mode ( $\overline{RE} = 0$ )	For Write Mode ( $\overline{WE} = 0$ )	$\overline{DAL}_7$ to $\overline{DAL}_0$ / $DAL_7$ to $DAL_0$
1	*	*	Deselected	Deselected	High Impedance
0	0	0	Status Register (STR)	Command Register (CR)	Enabled
0	0	1	Track Register (TR)	Track Register (TR)	Enabled
0	1	0	Sector Register (SCR)	Sector Register (SCR)	Enabled
0	1	1	Data Register (DR)	Data Register (DR)	Enabled

Pins 7 through 14,  $\overline{DAL}_0$  thru  $\overline{DAL}_7$  /  $DAL_0$  thru  $DAL_7$  (Data Bus)

These eight lines are an 8-bit bidirectional bus which is used to transfer 8-bit data between this FDC device and an connected MPU.

When  $\overline{CS} = 1$ , the bus is in the three-state.

All data are inverted, i.e. negative logic for MB8866 and MB8876.

All data are true for MB8877.

Pin 24, CLK (Clock)

This input is used as a standard clock signal. The clock frequency is usually 2MHz, but 1MHz for a mini-floppy disk.

Pin 38, DRQ (Data Request)

This output indicates a status of the DR.

In the read operation,  $DRQ = 1$  shows the DR is filled with a byte data so that the MPU can read the data.

In the write operation,  $DRQ = 1$  shows the DR is empty, i.e. this FDC device is requesting for the MPU to write a byte data into the DR.

The DRQ bit is reset by completion of the read or write operation.

This terminal is open-drain and externally pulled up with a 10k $\Omega$  resistor.

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## MPU Interface Pins Cont'd

### Pin 39, INTRQ (Interrupt Request)

This output indicates an interrupt status.

The INTRQ bit goes high when a Command is completed or stopped or the Type IV Command is executed.

This bit is reset when the next Command is written or the STR is read.

This terminal is open-drain and externally pulled up with a 10k $\Omega$  resistor.

### Pin 37, $\overline{\text{DDEN}}$ (Double Density)

This input is used to select a single density operation or a double density operation.

When  $\overline{\text{DDEN}} = 0$ , a double density operation mode is selected and vice versa.

## Floppy Disk Interface Pins

### Pin 15, STEP (Step Move)

This output pin provides a step pulse signal to drive a disk head.

One pulse drives one step motion.

### Pin 16, DIRC (Direction)

This output indicates a direction of disk head moving. DIRC = 0 shows the head moves toward outside while DIRC = 1 shows the head moves toward inside.

### Pin 17, EARLY (Early Shift)

This output is used for pre-compensation of data write timing to a disk.

EARLY = 1 indicates that a serial data to be transmitted from the WD (Write Data) pin to a disk must be shifted earlier.

### Pin 18, LATE (Late Shift)

This output is used for pre-compensation of data write timing to a disk.

LATE = 1 indicates that a serial data to be transmitted from the WD (Write Data) pin to a disk must be shifted later.

### Pin 23, HLT (Head Load Timing)

This input is used to recognize that a disk head has been settled or a pre-determined head settle time has elapsed after HLD = 1.

HLT = 1 shows a disk head is in an engaged state.

### Pin 25, RG (Read Gate)

This output is used to inform synchronization to an external data separator.

RG = 1 indicates that the FDC device has detected "0" — only data or "1" — only data on a disk, i.e. the FDC device has found out a SYNC byte in a ID field of disk.

### Pin 26, RCLK (Read Clock)

This input is used as a clock signal which defines data interval, i.e. data window.

This signal is externally generated corresponding to a stream of data and input to the FDC device. Signal levels "H" and "L" are not important but its falling and rising edges are essential.

### Pin 27, $\overline{\text{RAWREAD}}$ (Raw Read)

This input pin receives raw data transferred from a disk drive.

A data is given as a negative pulse.

### Pin 28, HLD (Head Load)

This output is used to control a motion of disk head.

When HLD = 1, the head is pressed on the media (disk).

When HLD = 0, the head is separated from the media (disk).

### Pin 29, TG43 (Track Greater Than 43)

This output indicates a head position on a disk.

When TG43 = 1, the head is located on any of Track No. 44 thru Track No. 76.

When TG43 = 0, the head is located on any of Track No. 0 thru Track No. 43. This signal is valid only for a Read Command or Write Command.

## MB8866 / MB8876 / MB8877

### MPU Interface Pins Cont'd

#### Pin 30, WG (Write Gate)

This output indicates that data is being written into a disk.

When data is being written into a disk, WG goes high.

#### Pin 31, WD (Write Data)

This input pin transmits a data to a disk. A data signal is a 250ns pulse for the MFM mode or a 500ns pulse for the FM mode.

#### Pin 32, READY (Ready)

This input pin receives a status of disk drive.

READY = 1 shows that the disk drive is ready for operation. Therefore, only when READY = 1, read or write operation for the disk can be executed.

When READY = 0, i.e. the disk drive is not ready, neither read or write operation can be executed and INTRQ goes high.

However, seek operation is executed regardless of this signal.

This input appears in NOT READY flag (Bit 7 of STR: STR 7) as negative copy, i.e. the STR 7 bit goes high when READY = 0.

#### Pin 33, $\overline{WF}/\overline{VFOE}$ (Write Fault/Variable Frequency Oscillator Enable)

This pin is used as both input and output modes, i.e. the Write Fault input and VFO Enable output. These modes are distinguished by the WG (Write Gate) output.

When WG = 1, i.e. the FDC device is writing data into a disk, this terminal acts as the Write Fault input.

If a fault of writing is detected during WG = 1 i.e.  $\overline{WF}$  goes low, the FDC device terminates the write operation by setting the WRITE FAULT flag (Bit 5 of STR: STR 5).

When WG = 0, i.e. the FDC device is not writing data into a disk, this terminal acts as the VFO Enable output.  $\overline{VFOE} = 0$  indicates that the FDC device is reading a disk. This terminal is open-drain port so that wire-dot connection is allowed.

#### Pin 34, $\overline{TR00}$ (Track 00)

This input indicates whether a disk head is positioned on Track No. 00 or not.

$\overline{TR00} = 0$  shows that Track No. 00 is detected during seeking operation.

#### Pin 35, $\overline{IP}$ (Index Pulse)

This input indicates that an index hole of disk is detected.

$\overline{IP} = 0$  shows the index hole is found out.

#### Pin 36, $\overline{WRPT}$ (Write Protect)

This input is used to inhibit write operation for a disk. This input is continuously sampled after a Write Command is initiated.

When  $\overline{WRPT} = 0$ , the Write Command execution is stopped and the WRITE PROTECT flag (Bit 6 of the STR: STR 6) is set reversly, i.e. the STR 6 bit goes high when  $\overline{WRPT} = 0$ .

### Other Pins

#### Pins 1 and 40

These pins are not used, i.e. No-Contact pins.

#### Pin 19, $\overline{MR}$ (Master Reset)

This input is used for resetting the FDC device.

When  $\overline{MR} = 0$ , the master reset procedure is initiated and then the STR 7 bit is reset to "0", the SEctor Register (SCR) is loaded with (01)H and the Command Register (CR) is loaded with (03)H.

At a rising edge of  $\overline{MR}$ , the Restore Command starts to be executed.

#### Pin 20, Vss (Power Supply)

This input is the Ground (GND) terminal.

#### Pin 21, Vcc (Power Supply)

This input is the +5V Power Supply terminal.

#### Pin 22, $\overline{TEST}$ (Test)

This input is used to set the FDC device into a test mode.

When  $\overline{TEST} = 0$ , the internal timer is ignored.

In a usual operation, this pin shall be connected to the +5V power supply or remain open.

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BIT STRUCTURES OF COMMANDS

MB8866

		(MSB) Command Register (CR) Bit (LSB)							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Seek	0	0	0	1	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step	0	0	1	u	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step In	0	1	0	u	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step Out	0	1	1	u	h	V	r <sub>1</sub>	r <sub>0</sub>
II	Read Data	1	0	0	m	X	E	0	0
II	Write Data	1	0	1	m	X	E	X	a <sub>0</sub>
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	X
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	l <sub>3</sub>	l <sub>2</sub>	l <sub>1</sub>	l <sub>0</sub>

X: Don't care  
Other alphabets: Flags which are used as parameters to specify various operation modes.

MB8876 / MB8877

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Seek	0	0	0	1	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step	0	0	1	u	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step In	0	1	0	u	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step Out	0	1	1	u	h	V	r <sub>1</sub>	r <sub>0</sub>
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a <sub>0</sub>
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	l <sub>3</sub>	l <sub>2</sub>	l <sub>1</sub>	l <sub>0</sub>

NOTE: Bits shown in TRUE form.

TABLE 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	X	X
R1 R0	TEST = 1	TEST = 1	TEST = 1	TEST = 1	TEST = 0	TEST = 0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

TYPE I COMMANDS

**h = Head Load Flag (Bit 3)**  
h = 1, Load head at beginning  
h = 0, Unload head at beginning

**V = Verify flag (Bit 2)**  
V = 1, Verify on destination track  
V = 0, No verify

**r<sub>1</sub>r<sub>0</sub> = Stepping motor rate (Bits 1-0)**  
Refer to Table 1 for rate summary

**u = Update flag (Bit 4)**  
u = 1, Update Track register  
u = 0, No update

TYPE II & III COMMANDS

**m = Multiple Record flag (Bit 4)**  
m = 0, Single Record  
m = 1, Multiple Records

**a<sub>0</sub> f = Data Address Mark (Bit 0)**  
a<sub>0</sub> = 0, FB (Data Mark)  
a<sub>0</sub> = 1, F8 (Deleted Data Mark)

**E = 15 ms Delay (2MHz)**  
E = 1, 15 ms delay  
E = 0, no 15 ms delay

**S = Side Select Flag**  
S = 0, Compare for Side 0  
S = 1, Compare for Side 1

**C = Side Compare Flag**  
C = 0, disable side select compare  
C = 1, enable side select compare

TYPE IV COMMAND

**li = Interrupt Condition flags (Bits 3-0)**  
l<sub>0</sub> = 1, Not-Ready to Ready Transition  
l<sub>1</sub> = 1, Ready to No-Ready Transition  
l<sub>2</sub> = 1, Index Pulse  
l<sub>3</sub> = 1, Immediate Interrupt  
l<sub>3</sub> - l<sub>0</sub> = 0, Terminate with no Interrupt

**ELECTRICAL CHARACTERISTICS**

**GUARANTEED OPERATING CONDITIONS**

(Referenced to V<sub>SS</sub>)

Parameter	Symbol	Value			Unit	Operating Temperature
		min	typ	min		
Supply Voltage	V <sub>CC</sub>	4.75	5.00	5.25	V	0°C to +70°C
Supply Voltage	V <sub>SS</sub>	—	0	—	V	
Input High Voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub>	V	
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V	

**DC CHARACTERISTICS**

(Full Guaranteed Operating Conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		min	typ	max	
Output High Voltage (I <sub>OH</sub> = -200 A)	V <sub>OH</sub>	2.4	—	—	V
Output Low Voltage (I <sub>OL</sub> = 1.8mA)	V <sub>OL</sub>	—	—	0.4	V
Three-State (Off-State) Input Current (V <sub>IN</sub> = 0.4V to 2.4V)	I <sub>TSI</sub>	—	—	10	μA
Input Leakage Current (See Note 1)	I <sub>IN</sub>	—	—	2.5	μA
Output Leakage Current for Off-State (V <sub>OH</sub> = 2.4V)	I <sub>LOH</sub>	—	—	10	μA
Power Consumption	P <sub>C</sub>	—	300	350	mW

NOTE 1) Except for HLT, TEST, WF, WPRT, and DDEN. (V<sub>IN</sub> = 0 to 5.25V)

**AC CHARACTERISTICS**

(Full Guaranteed Operating Conditions unless otherwise noted.)

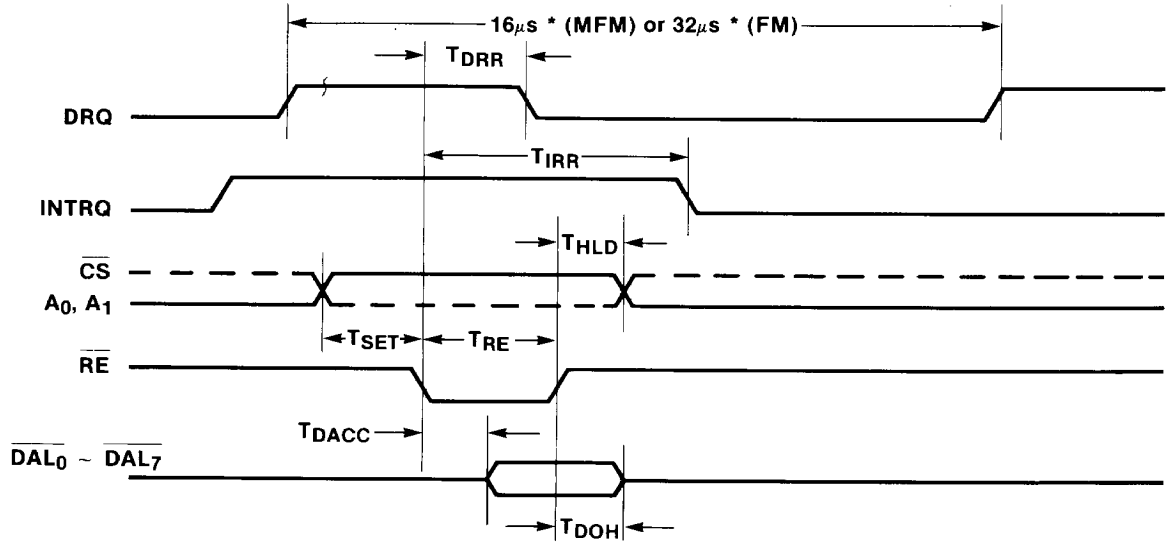
**MPU Read Timing**

Parameter	Symbol	Value			Unit
		min	typ	max	
Address Setup Time	t <sub>SET</sub>	0	—	—	ns
Address Hold Time	t <sub>HLD</sub>	10	—	—	ns
RE Pulse Width (C <sub>L</sub> = 25pF)	t <sub>RE</sub>	400	—	—	ns
DRQ Reset Time	t <sub>DRR</sub>	—	—	500	ns
INTRQ Reset Time	t <sub>IRR</sub>	—	500*	3000*	ns
Data Delay Time (C <sub>L</sub> = 25pF)	t <sub>DACC</sub>	—	—	350	ns
Data Hold Time (C <sub>L</sub> = 25pF)	t <sub>DOH</sub>	50	—	150	ns

\*: These values are doubled when CLK = 1MHz.



**READ TIMING DIAGRAM**

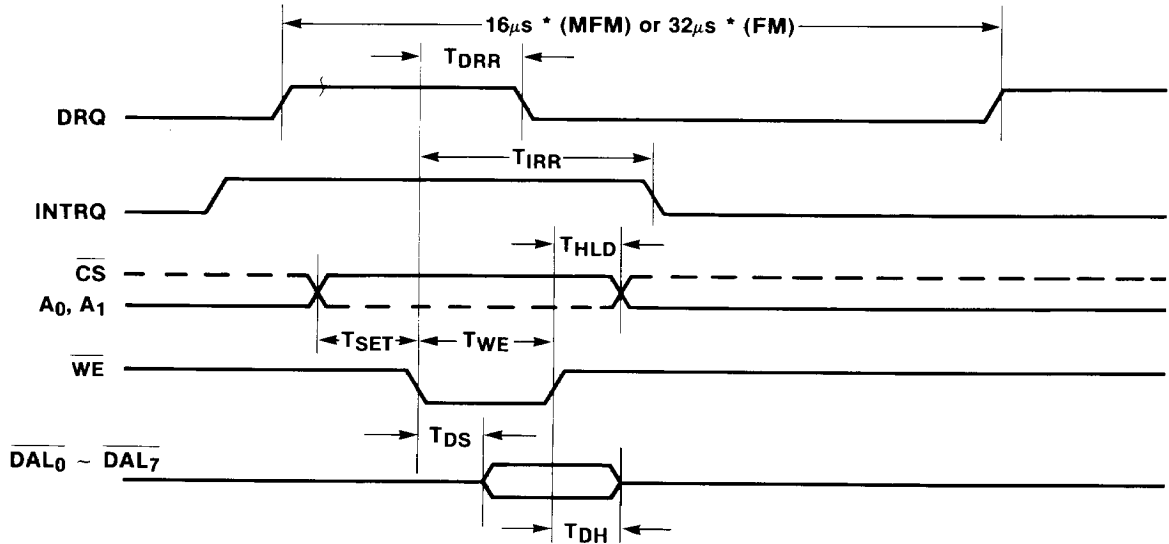


**MPU Write Timing**

Parameter	Symbol	Value			Unit
		min	typ	max	
Address Setup Time	t <sub>SET</sub>	0	—	—	ns
Address Hold Time	t <sub>HLD</sub>	10	—	—	ns
$\overline{WE}$ Pulse Width	t <sub>WE</sub>	350	—	—	ns
DRQ Reset Time	t <sub>DRR</sub>	—	—	500	ns
INTRQ Reset Time	t <sub>IRR</sub>	—	500*	3000*	ns
Data Setup Time	t <sub>DS</sub>	250	—	—	ns
Data Hold Time	t <sub>DH</sub>	65	—	—	ns

\*: These values are doubled when CLK = 1MHz.

**WRITE TIMING DIAGRAM**

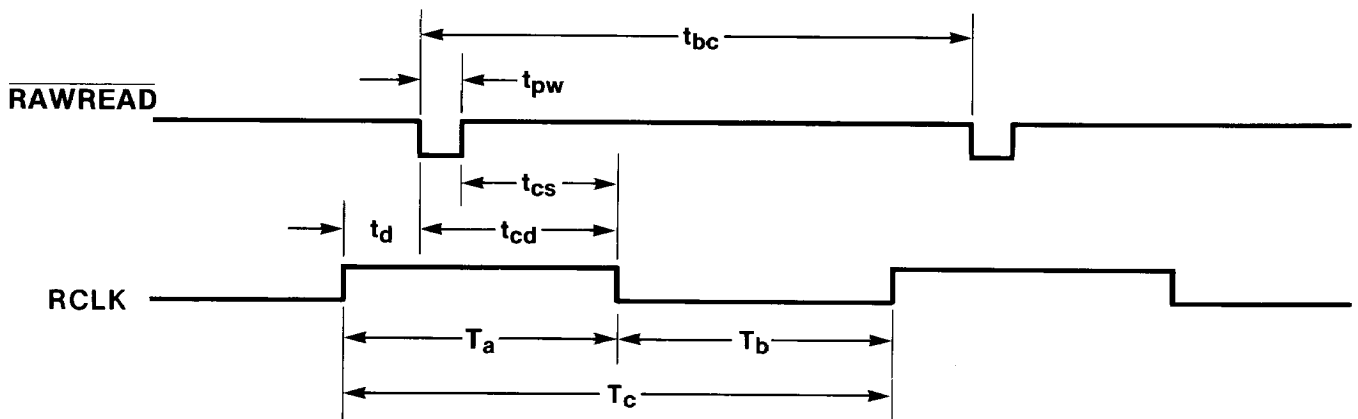


**DISK INPUT DATA TIMING**

Parameter		Symbol	Value			Unit
			min	typ	max	
RAWREAD Pulse Width		$t_{pw}$	100*	—	250*	ns
Clock Setup Time		$t_d$	40	—	—	ns
Clock Hold Time for MFM		$t_{cd}$	40	—	—	ns
Clock Hold Time for FM		$t_{cs}$	40	—	—	ns
RAWREAD Cycle Time	MFM	$t_{bc}$	—	2*, 3* or 4*	—	$\mu S$
	FM		—	2* or 4*	—	$\mu S$
RCLK High Pulse Width	MFM	$t_a$	0.8	1*	—	$\mu S$
	FM		0.8	2*	—	$\mu S$
RCLK Low Pulse Width	MFM	$t_b$	0.8	1*	—	$\mu S$
	FM		0.8	2*	—	$\mu S$
RCLK Cycle Time	MFM	$t_c$	—	2*	—	$\mu S$
	FM		—	4*	—	$\mu S$

\*: These values are doubled when CLK = 1MHz.

**DISK INPUT TIMING**

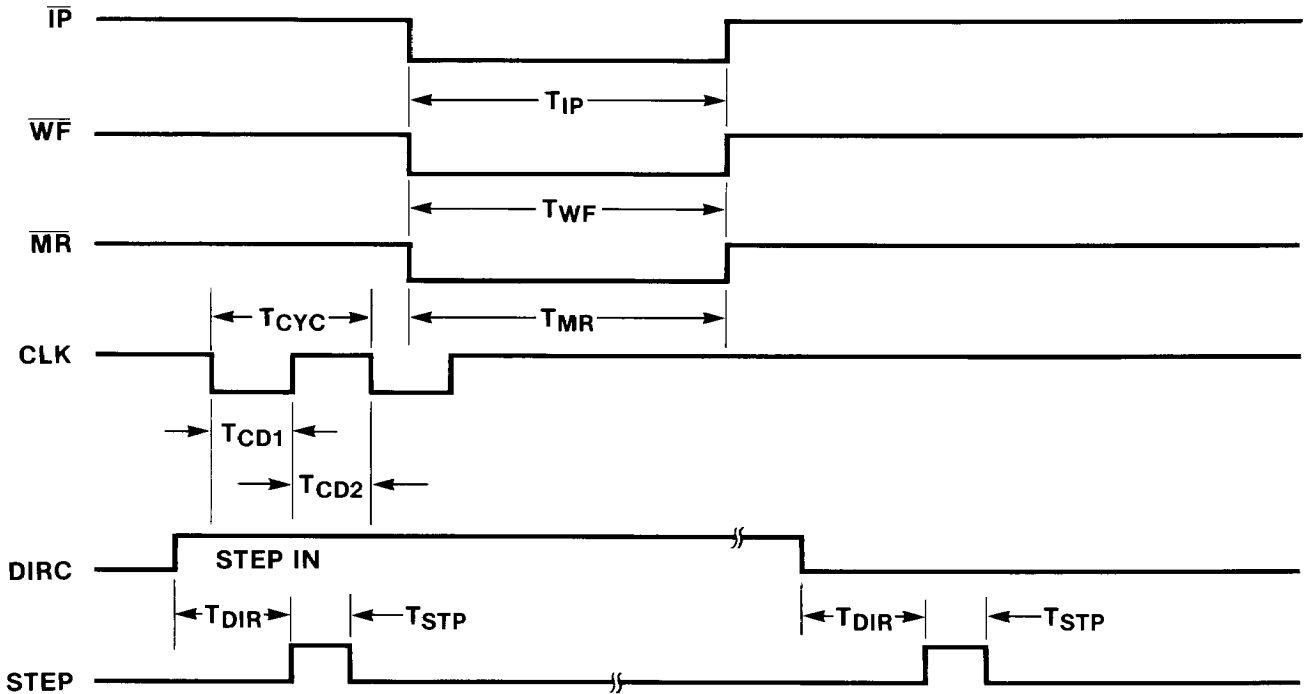


OTHER TIMINGS

Parameter	Symbol	Value			Unit
		min	typ	max	
CLK Low Pulse Width	$t_{CD1}$	230	—	—	ns
CLK High Pulse Width	$t_{CD2}$	200	—	—	ns
STEP Pulse Width	MFM	2*	—	—	$\mu$ S
	FM	4*	—	—	$\mu$ S
DIRC Setup Time	$t_{DIR}$	12*	—	—	$\mu$ S
MR Pulse Width	$t_{MR}$	50*	—	—	$\mu$ S
$\overline{IP}$ Pulse Width	$t_{IP}$	10*	—	—	$\mu$ S
WF Pulse Width	$t_{WF}$	10*	—	—	$\mu$ S
CLK Cycle Time	$t_{CYC}$	—	0.5*	—	$\mu$ S

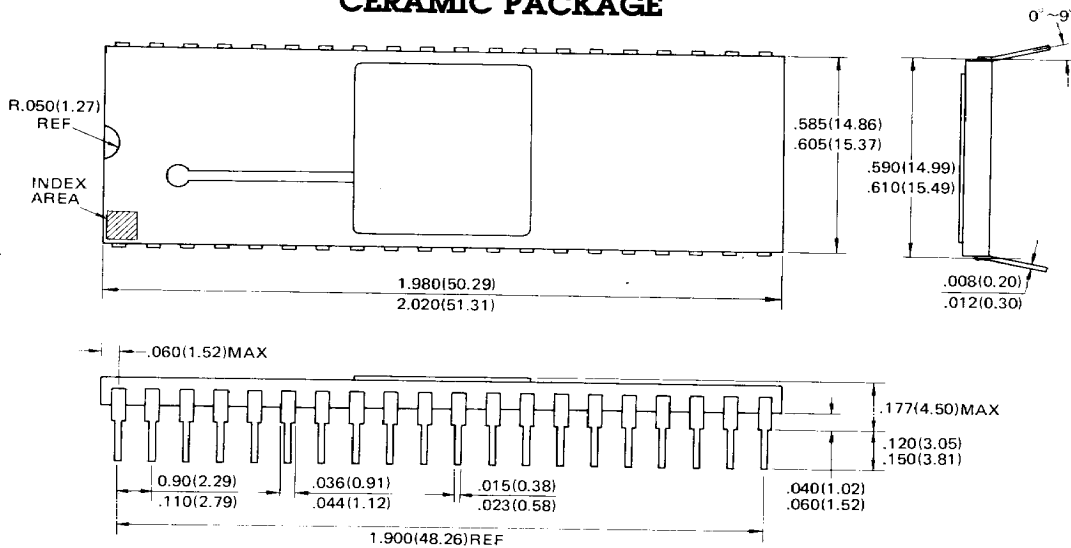
\*: These Values are doubled when CLK = 1MHz.

TIMING DIAGRAM

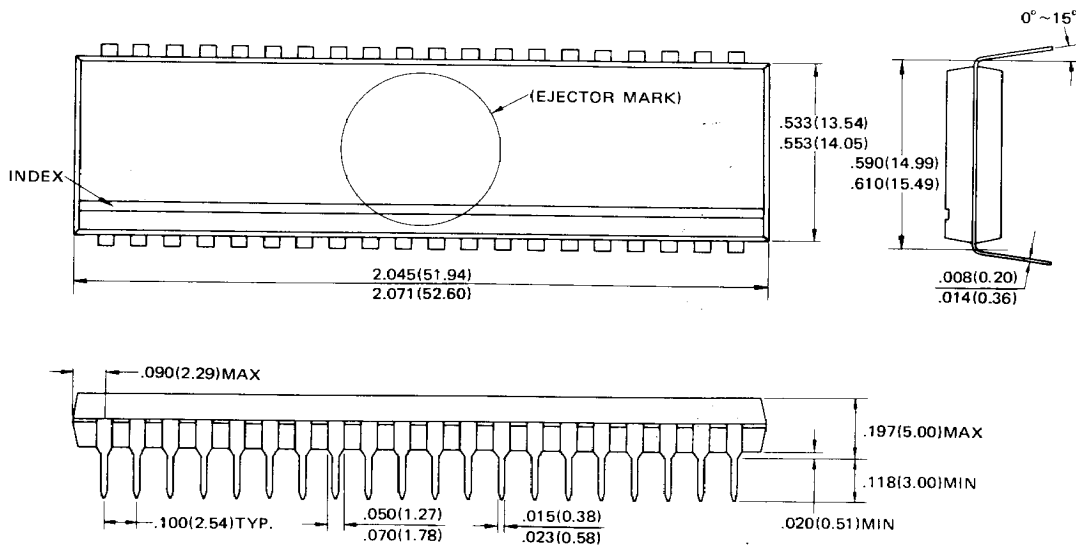


**PACKAGE DIMENSIONS** Dimensions in inches (millimeters)

**DIP-40C-A01  
CERAMIC PACKAGE**



**DIP-40P-M01  
PLASTIC PACKAGE**



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